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## Electrical transport in high-quality graphene *pnp* junctions

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**Abstract.** We fabricate and investigate high-quality graphene devices with contactless, suspended top gates and demonstrate the formation of graphene *pnp* junctions with tunable polarity and doping levels. The device resistance displays distinct oscillations in the *npn* regime, arising from the Fabry–Perot interference of holes between the two *pn* interfaces. At high magnetic fields, we observe well-defined quantum Hall plateaus, which can be satisfactorily fit to theoretical calculations based on the aspect ratio of the device.

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### 1. Introduction

Graphene [1]–[3] is a two-dimensional allotrope of carbon with a unique linear dispersion relation for low-lying excitations. Its gapless electronic band structure allows continuous tuning of charge carrier type and density by an electrostatic gate. Thus, one of the unique device

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configurations enabled by graphene is a dual-gated device, in which two or more gates are used to individually control charge density in different regions, realizing, for instance, *pn*p or *n*pn junctions with *in situ* tunable junction polarity and doping levels [4]–[6]. Such *pn*p junctions have been demonstrated experimentally [7]–[14], offering unique platforms for investigation of novel phenomena such as Klein tunneling [15, 16], particle collimation [4, 17], anisotropic transmission [18] and Veselago lensing effects [19].

Here we report fabrication of high-quality *pn*p junctions using suspended, contactless top gates. Distinct resistance oscillations in the bipolar region are observed, arising from Fabry–Perot interference of holes between the two *pn* interfaces. At high magnetic fields, device conductance displays quantum Hall plateaus at fractional values of  $e^2/h$ , as a result of edge state equilibration. Using a recently available theory for rectangular device geometry [20], we can satisfactorily account for the two-terminal device conductance at uniform charge densities.

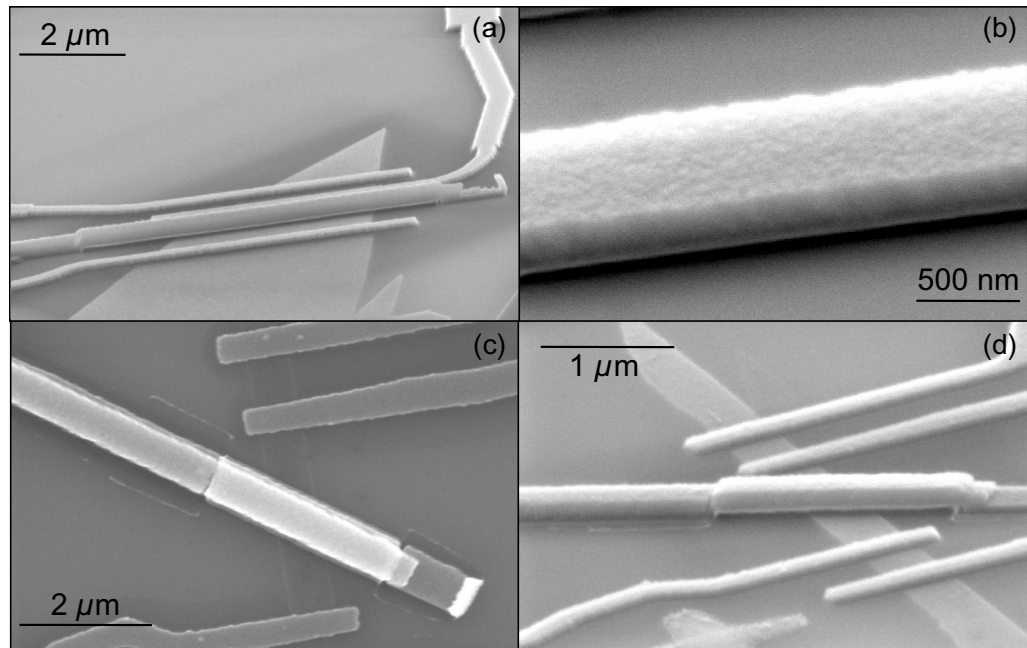
## 2. Device fabrication

Because graphene consists of only one atomic layer of carbon, deposition of top gate materials may introduce defects, dopants or additional scattering sites, thus reducing the device mobility. Previously, electron beam resists [8, 10] or alternating layers of NO<sub>2</sub>, trimethylaluminum and Al<sub>2</sub>O<sub>3</sub> [9] have been used as the dielectrics for local gates. We have recently developed a multi-level lithography technique to fabricate ‘air-bridge’-styled top gates, in which a metallic bridge is suspended across part of the graphene sheet, with vacuum acting as the dielectric. A similar technique was also reported by Gorbachev *et al* [12]. Since graphene is only exposed to conventional lithographical resists and developers during fabrication, this technique minimizes the damage to the atomic layer. It is also compatible with post-fabrication annealing [21, 22], which improves device mobility by removing resist residuals and adsorbates on the graphene surface, including those from the region directly under the top gate.

The substrate consists of a 300 nm SiO<sub>2</sub> layer grown over degenerately doped silicon, which can serve as a global back gate. Graphene sheets are deposited onto the substrate by the standard micro mechanical exfoliation method [1], and we identify the number of layers in a given sheet by color contrast in an optical microscope and Raman spectroscopy [23]. To fabricate the air bridge, we employ a resist bilayer with different exposure and developing conditions, so as to create a temporary support for the suspended structure; this resist support is subsequently removed after double-angle metal depositions at  $-45^\circ$  and  $45^\circ$ . The details of fabrication are discussed in [11]. Finally, using standard electron beam lithography, we deposit electrodes, consisting of 10 nm of Ti and 80 nm of Al, on graphene. The height of the air gap depends on the thickness of resists, and is as small as 50 nm for our devices (figures 1(a) and (b)). **To ensure suspension of the air bridge over distances as long as 12  $\mu$ m, a critical point dryer is typically used during fabrication of the top gate and electrodes.**

The suspended gates can also be fabricated at nonzero angles with respect to the source–drain electrodes (figures 1(c) and (d)), by careful control of the direction of metal evaporations. Such graphene devices with angled top gates were first proposed in [15], as an experimental platform to observe Klein tunneling, in which the transmission coefficient of charges across high potential barriers strongly depends on the incident angle.

The most common failure mechanism of a suspended bridge is its collapse under sufficiently high voltages. Our previously fabricated device typically failed at critical voltages of  $\sim 40$ – $60$  V, due to the poor contacts between the vertical sidewalls and the horizontal bridge and



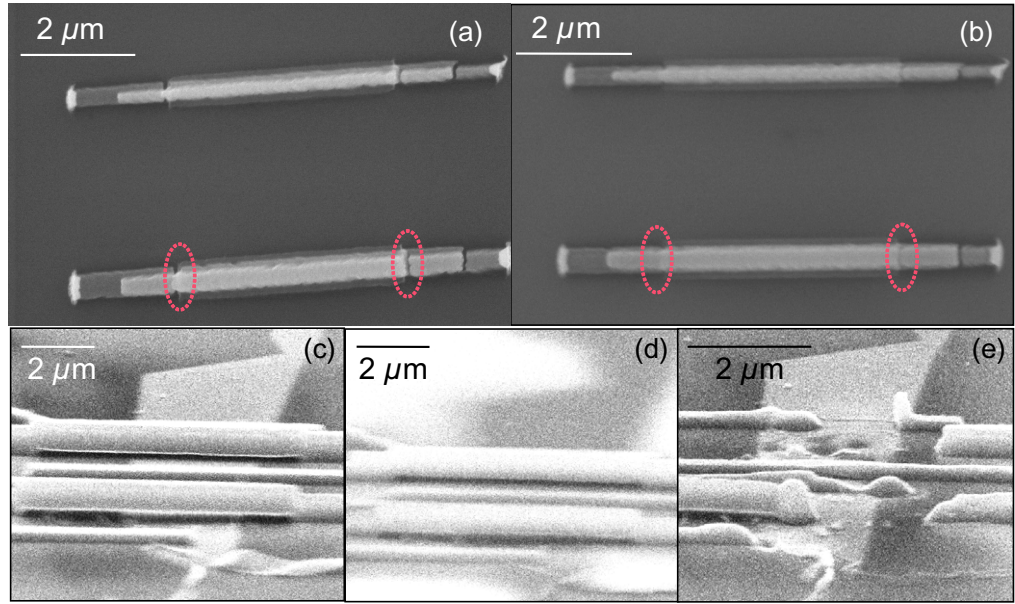
**Figure 1.** SEM images of suspended top gates. (a) A completed graphene device with a top gate suspended  $\sim 100$  nm above the substrate. (b) Image of the top gate suspended at 50 nm above the substrate. (c, d) A graphene device with a suspended top gate that is not parallel to the electrodes. The images are taken at tilt angles of  $0^\circ$  and  $70^\circ$ , respectively.

electrodes. To overcome this deficiency, we perform an additional evaporation at  $0^\circ$ . Figures 2(a) and (b) show two sets of suspended air bridges fabricated with two and three angle evaporations, respectively. Compared with figure 2(a), the ‘joints’ between different segments (outlined by dotted circles) in figure 2(b) are visibly strengthened.

To verify the mechanical robustness of these structures, we perform *in situ* scanning electron microscope (SEM) imaging, while applying voltages to the top gate. As shown by the images in figures 2(c)–(e), the air bridge remains suspended and undeformed under voltages of 70 and 100 V, and ultimately fails at 110 V. This surprisingly high critical voltage demonstrates significant improvement over our previous top gate structures.

### 3. Conductance of a *pnp* junction at $B = 0$

Transport measurements on the graphene devices are performed at 260 mK in a He<sup>3</sup> fridge using standard lock-in techniques. By varying voltages applied to the back gate (that controls the charge density and type in the entire device) and to the top gate (that controls charges directly under it), a graphene *pnp* junction can be created. A typical data set is shown in figure 3(a), plotting the four-terminal device resistance  $R$  (color) as functions of  $V_{bg}$  (the vertical axis) and top-gate voltage  $V_{tg}$  (the horizontal axis). The source–drain separation  $L$  of the device is  $3.5 \mu\text{m}$ , and width  $W$  is  $1 \mu\text{m}$ . The top gate is suspended  $d \sim 100$  nm above the center segment of graphene, with a length  $L_{tg} \approx 0.5 \mu\text{m}$ . In the non-top-gated or ‘bare’ regions of the device,



**Figure 2.** (a) SEM images of suspended test structures fabricated with double-angle evaporations (at  $-45^\circ$  and  $45^\circ$ ). The red circles indicate the weak points of the structure. (b) Same as (a), but fabricated with triple-angle evaporations (at  $-45^\circ$ ,  $45^\circ$  and  $0^\circ$ ). The weak points are visibly reinforced. (c, e) SEM images of a suspended top gate under applied voltages of 70, 100 and 110 V, respectively.

the charge density  $n_1$  is modulated by  $V_{\text{bg}}$  only,

$$n_1 = C_{\text{bg}}(V_{\text{bg}} - V_{\text{D,bg}})/e, \quad (1a)$$

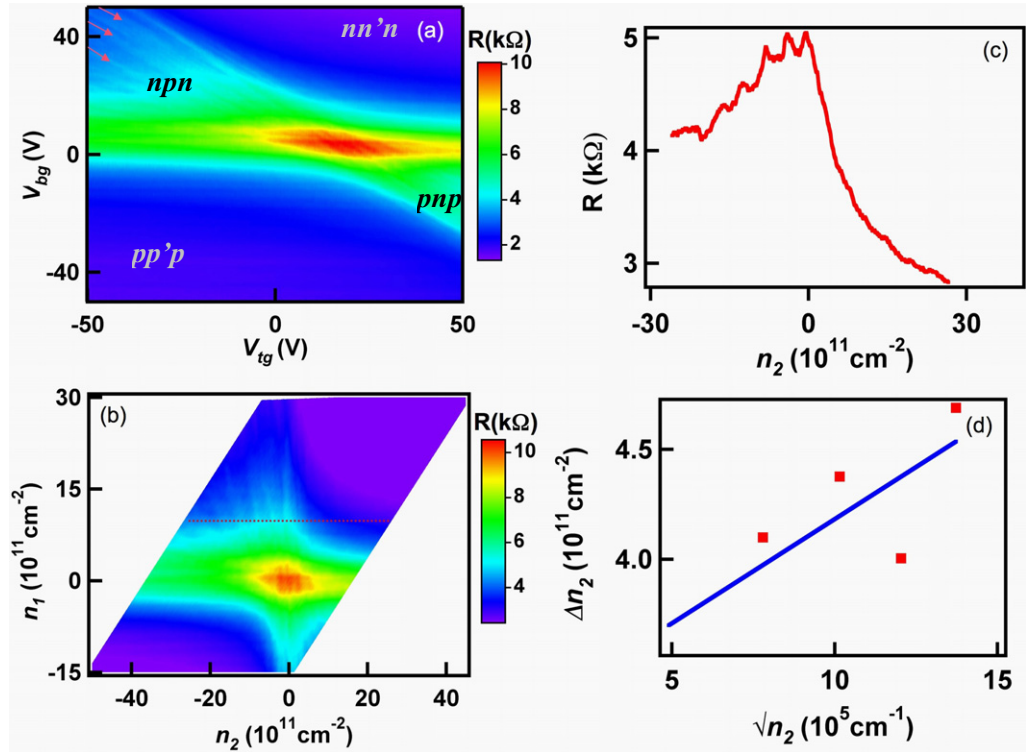
where  $e$  is the electron's charge,  $C_{\text{bg}}$  is the capacitance per unit area between graphene and the back gate, and  $V_{\text{D,bg}}$  is the Dirac point of the bare region of the device, which may be nonzero due to doping by contaminants. From figure 3(a),  $V_{\text{D,bg}} \sim 3.5$  V, at which device resistance reaches a maximum; since these regions account for 85% of the device area, their responses dominate the device resistance, yielding the horizontal green–red band.

For the top-gated or ‘covered’ region, the charge density  $n_2$  is modulated by both  $V_{\text{bg}}$  and  $V_{\text{tg}}$

$$n_2 = n_1 + C_{\text{tg}}(V_{\text{tg}} - V_{\text{D,tg}})/e. \quad (1b)$$

At  $n_1 = 0$ , the resistance maximum occurs at the Dirac point of the top-gated region,  $V_{\text{D,tg}} \sim 18$  V. The diagonal cyan line, indicating a local resistance maximum, corresponds to the charge neutrality point of the region directly under the top gate, i.e.  $n_2 = 0$ . Its slope thus yields the capacitance or gate coupling ratio,  $\eta = C_{\text{tg}}/C_{\text{bg}}$ , measured from the figure to be  $\sim 0.78$ . This is in good agreement with the value estimated from geometrical considerations,  $C_{\text{tg}}/C_{\text{bg}} = (\varepsilon_{\text{tg}}/\varepsilon_{\text{bg}})(d_{\text{bg}}/d_{\text{tg}}) \approx (1/3.9)(300/100) = 0.77$ , where  $\varepsilon$  is the dielectric constant of the gate, and  $d$  is the device–gate separation. Taken together, the horizontal band of  $n_1 = 0$ , together with the cyan diagonal line of  $n_2 = 0$ , partition the data in figure 3(a) into four regions, with different doping combinations, thus demonstrating a graphene *pnp* junction with *in situ* tunable polarity and doping levels.





**Figure 3.** Data in zero magnetic field. (a) Four-terminal device resistance as functions of  $V_{bg}$  and  $V_{tg}$ . The arrows indicate oscillations in the  $npn$  region. (b) Same data as (a), but plotted against  $n_2$  and  $n_1$ . (c) Line trace along the dotted line in (b), showing resistance oscillation as a function of  $n_2$ . (d) The peak spacing  $\Delta n_2$  versus  $\sqrt{n_2}$ . The line represents a linear fit to the data.

We now focus exclusively on the upper left region of figure 3(a), i.e. when the junction is in the  $npn$  regime. Compared with the neighboring unipolar ( $pp'p$  or  $nn'n$ ) regions, the junction resistance is significantly higher, as expected at the boundary of a  $pn$  junction. More interestingly, we observe resistance oscillations as a function of both  $V_{bg}$  and  $V_{tg}$ , as indicated by the arrows in figure 3(a). Notably, these oscillations are not found in the unipolar regions. Such oscillations were first reported by Young and Kim [13], and arise from Fabry–Perot interference of the charges between the two  $p$ – $n$  interfaces. Thus, the holes in the top-gated region are multiply reflected between the two interfaces, interfering to give rise to standing waves, similar to those observed in carbon nanotubes [24] or standard graphene devices [25]. Modulations in  $n_2$  change the Fermi wavelength of the charge carriers, hence altering the interference patterns and giving rise to the resistance oscillations.

To analyze these oscillations in detail, we replot the data in figure 3(a) in terms of  $n_1$  and  $n_2$ . Assuming a parallel plate geometry between the gate and the device,  $C_{bg}/e \approx 7.19 \times 10^{10} \text{ cm}^{-2}$ . However, from quantum Hall measurements, we estimate the effective capacitance to be  $\sim C_{bg}/e \approx 6.51 \times 10^{10} \text{ cm}^{-2}$  (see discussion in the next section). This small discrepancy may be attributed to a slightly thicker  $\text{SiO}_2$  layer, slightly smaller  $\epsilon_{bg}$ , or additional screening by the electrodes. Using this value, we have

$$n_1 = 6.5 \times 10^{10} (V_{bg} - V_{D,bg}) \text{ cm}^{-2} \quad (2a)$$

and

$$n_2 = 6.5 \times 10^{10} [(V_{\text{bg}} - V_{\text{D,bg}}) + \eta(V_{\text{tg}} - V_{\text{D,tg}})] \text{ cm}^{-2}. \quad (2b)$$

The new plot is shown in figure 3(b). The color scale is adjusted to accentuate the resistance oscillations, which appear as fringes fanning out from the Dirac point at  $n_1 = n_2 = 0$ . Figure 3(c) shows the device resistance versus  $n_2$  at  $n_1 = 1.3 \times 10^{12} \text{ cm}^{-2}$ , displaying clear oscillations.

Within the Fabry–Perot model, the resistance peaks correspond to minima in the overall transmission coefficient; the peak separation can be approximated by the condition  $k_{\text{F}}(2L_c) = 2\pi$ , i.e. a charge accumulates a phase shift of  $2\pi$  after completing a roundtrip  $2L_c$  in the cavity. Here  $k_{\text{F}}$  is the Fermi wave vector of the charges, and  $L_c$  is the length of the Fabry–Perot cavity. Under the top gate,  $k_{\text{F}2} = \sqrt{\pi n_2}$ , so the spacing between successive peaks is estimated to be

$$\Delta n_2 \approx \frac{4\sqrt{\pi n_2}}{L_c}. \quad (3)$$

In figure 3(d), we plot the measured peak spacing for the curve shown in figure 3(c) against  $\sqrt{n_2}$ . The data points fall approximately on a straight line. The best linear fit yields a line with a slope  $0.95 \times 10^5 \text{ cm}^{-1}$ , corresponding to  $L_c = 740 \text{ nm}$  from equation (3). This agrees with the value estimated from electrostatics,  $L_c = L_{\text{tg}} + 2d$ , as the electric field induced by the top gate on the device is expected to extend by a distance  $\sim d$  away from either edge.

Finally, we note that the device in [13] had extremely narrow gates  $L_{\text{tg}} \lesssim 20 \text{ nm}$ . In comparison, our top gate spans a much larger distance,  $L_{\text{tg}} \sim 500 \text{ nm}$ . Thus, the observation of clear Fabry–Perot interference patterns underscores the high quality of our *pnp* graphene devices.

#### 4. Conductance of a *pnp* junction at $B = 8 \text{ T}$

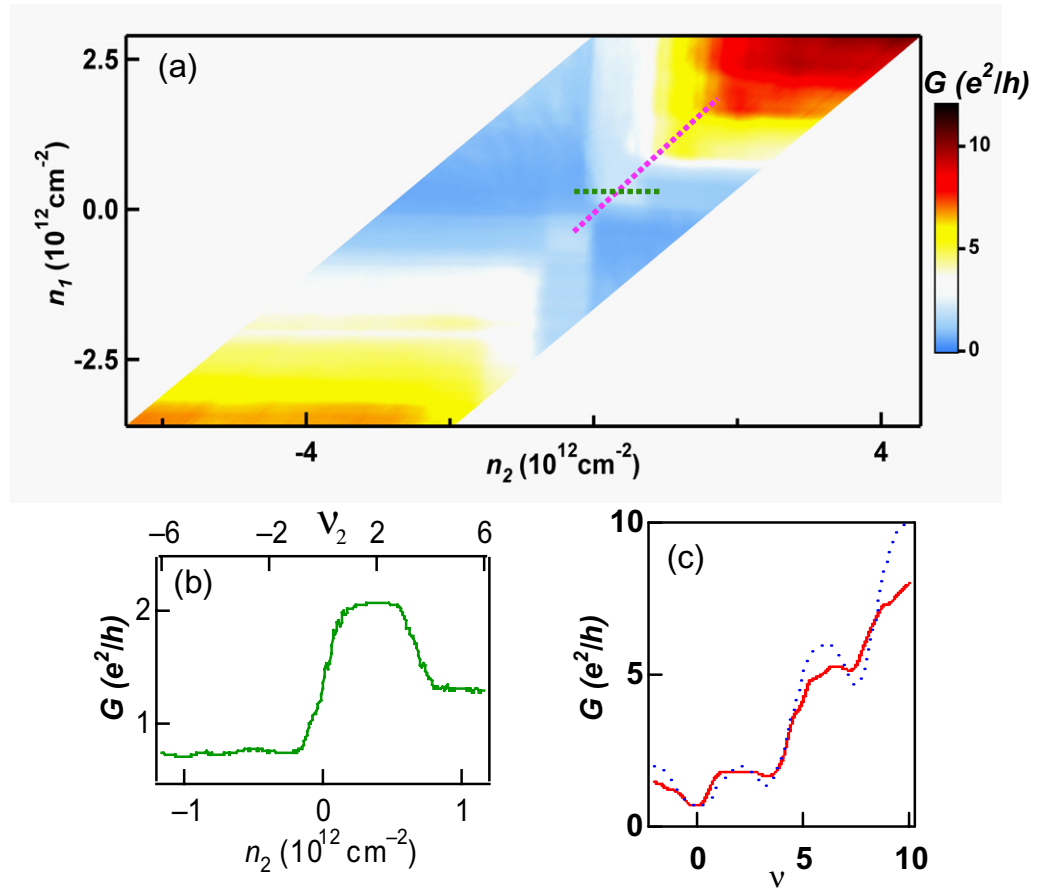
In high magnetic fields, the cyclotron orbits of charges coalesce to form Landau levels (LLs). For graphene with uniform charge densities, the energies of the LLs are given by  $E_N = \text{sgn}(N)\sqrt{2e\hbar v_{\text{F}}^2|N|B}$ , and the Hall conductivity is  $\sigma_{xy} = 4(N + \frac{1}{2})(e^2/h)$ , where  $N$  is an integer denoting the LL index,  $e$  is the electron charge,  $v_{\text{F}}$  is the Fermi velocity of charges in graphene,  $\hbar$  is Planck's constant. The factor of 4 arises from the spin and sublattice degeneracies. A unique signature of graphene's linear dispersion relation is the presence of the zeroth LL that is shared equally by electrons and holes, leading to quantum Hall plateaus that are quantized at half-integer values of  $4e^2/h$  [1, 3].

For a graphene device with a dual gate, the situation is complicated by the presence of regions with different filling factors, or the co-existence of *n*- and *p*-doped regions that result in counter-propagating edge states. The two-terminal conductance of the junction depends on the relative values of  $n_1$  and  $n_2$ , and can have fractional values of  $e^2/h$ . A simple model is provided in [26], assuming perfect edge state equilibration at the interfaces between different regions: for a unipolar junction ( $n_1 n_2 > 0$ ) with  $|n_1| \geq |n_2|$ , the non-top-gated regions act as reflectionless contacts to the center region, yielding a device conductance

$$G = e^2/h|v_2|, \quad (4)$$

where  $v_1$  and  $v_2$  are the filling factors in the bare and top-gated regions, respectively, given by  $v = nh/Be$ , where  $B$  is the applied magnetic field. If instead  $|n_2| > |n_1|$ , the conductance is

$$G = \frac{e^2}{h} \left( \frac{1}{|v_1|} - \frac{1}{|v_2|} + \frac{1}{|v_1|} \right)^{-1}. \quad (5)$$



**Figure 4.** Data at  $B = 8$  T. (a) Two-terminal device conductance  $G$  versus  $n_1$  and  $n_2$ . (b) Line trace along the green dotted line  $\nu_1 = 2$  in (a). (c) The solid red curve is a line trace taken along the magenta dotted line  $n_2 = n_1$  in (a). The dotted line is a theoretical curve calculated using the expressions in [20],  $L/W = 3.5$  and  $\Gamma = 0.67$ , where  $\Gamma$  is a fitting parameter that describes the width of the longitudinal resistivity in density.

For a bipolar junction ( $n_1 n_2 < 0$ ), the device behaves simply as three resistors in series,

$$G = \frac{e^2}{h} \left( \frac{1}{|\nu_1|} + \frac{1}{|\nu_2|} + \frac{1}{|\nu_1|} \right)^{-1}. \quad (6)$$

From equations (4)–(6), the conductance of a graphene *pnp* junctions displays plateaus at fractional multiples of  $e^2/h$ . We emphasize that these fractional-valued plateaus are not related to the fractional quantum Hall effect; rather, they arise from the inhomogeneous filling factors within the device.

To observe these plateaus, we measure the two-terminal conductance  $G$  of the device as functions of  $V_{bg}$  and  $V_{tg}$  at  $B = 8$  T. The data are shown in figure 4(a), plotting  $G$  (color) versus  $n_1$  and  $n_2$ , which are calculated from gate voltages using equations (1) and (2). The conversion factor  $C_{bg}/e$  is obtained by noting that measured from the global Dirac point



( $n_1 = n_2 = 0$ ), the center of the first finite density plateau should occur at  $\nu = 2$  or  $n = 3.9 \times 10^{11} \text{ cm}^{-2}$  at 8 T; the corresponding gate voltage difference is 6 V, yielding an effective  $C_{\text{bg}}/e \sim 6.51 \times 10^{10} \text{ cm}^{-2} \text{ V}^{-1}$ . This value is  $\sim 9\%$  lower than that estimated from a simple parallel plate capacitor model, and is used for all plots in figures 3 and 4.

The data in figure 4(a) exhibit regular rectangular patterns, which arise from the filling of additional LLs as  $n_1$  and  $n_2$  are modulated. A line trace of  $G(n_2)$  at  $\nu_1 = 2$  is shown in figure 4(b), with equivalent values of  $\nu_2$  labeled on the top axis. As  $\nu_2$  varies from  $-2$ , 2 to 6, conductance plateaus with values of  $\sim 0.67$ , 2 and  $1.2e^2/h$  are observed, in excellent agreement with those obtained using equations (6)–(8). The solid line in figure 4(c) plots  $G(\nu)$  for uniform charge densities over the entire graphene sheet, i.e. along the diagonal dotted line  $n_2 = n_1$  in figure 4(a). The  $\nu = 2$  plateau is well developed, indicating relatively small amount of disorder.

We now focus on the small conductance dips in figure 4(c) at  $\nu \sim 3$  and 7, which are not expected to be present for a square device with  $L = W$ . Indeed, the two-terminal conductance of a conducting *square* includes both longitudinal and Hall conductivity signals,  $G = \sqrt{\sigma_{xx}^2 + \sigma_{xy}^2}$ , so  $G(\nu)$  appears as stepwise plateaus that increases monotonously for  $\nu > 0$ . However, for other device geometries the behaviors are more complicated. Depending on the aspect ratio of the device, the device conductance displays local conductance peaks or dips between the plateaus; if the device has significant LL broadening, the conductance will no longer be quantized at integer values of  $2, 6, 10, \dots, e^2/h$ . This was studied in detail in [20], using an effective medium approach that yields a semicircle relation between  $\sigma_{xx}$  and  $\sigma_{xy}$ . To quantitatively examine the agreement between the data and the theory, we model the longitudinal conductivity as a Gaussian centered at an LL,  $\delta_N \sigma_{xx}(\nu) = 2e^{-[\nu - 1/2(\nu_N + \nu_{N+1})]^2/\Gamma}$  in units of  $e^2/h$ . Here  $\nu_N = 4(N + \frac{1}{2})(|B|e/h)$  are the incompressible densities corresponding to the  $N$ th LL, and  $\Gamma$  describes the width of the Gaussian distribution. Following the procedures outlined in [20], and using a fitting parameter  $\Gamma = 0.67$ , we calculate  $G(\nu)$  for our rectangular device with aspect ratio  $L/W = 3.5$ . The resultant curve is shown as the dotted line in figure 4(c). The agreement with data is satisfactory at smaller values of  $\nu$ , but deviates for  $\nu > 6$ . This is quite reasonable, since the energetic difference between LL decreases for higher levels. Moreover, the value of  $\Gamma = 0.67$  obtained from the fitting is relatively small, again underscoring the high junction quality.

Finally, we note that the model leading to equations (4)–(6) is based on the single-particle picture and assumes perfect edge state equilibration at the interfaces between different regions. The excellent agreement between our experimental results and model validates this assumption. On the other hand, if the electrical transport is fully coherent, one expects to observe universal conductance fluctuations (UCF) instead of well-defined plateaus. The exact origin of such mode-mixing mechanism and suppression of UCF is not clear, but is likely related to the presence of disorder, and/or dephasing due to coupling of the edge states to localized states in the bulk. Thus, an interesting future direction to explore is the mode-mixing mechanism (or the lack thereof) by studying ultra-clean *pnp* junctions.

## 5. Conclusion

Using suspended top gates, we are able to fabricate high-quality *npn* junctions, which display Fabry–Perot resistance oscillations within a small cavity formed by the *pn* interfaces. In high magnetic fields, well-developed quantum Hall plateaus are observed, and the behavior can be

quantitatively described by theoretical predictions for rectangular device geometry. In the long term, this technique may be important for the study of transport of Cooper pairs [27]–[29] or spins [30, 31] through *pn* junctions or the experimental realization of on-chip electronic lenses [19], which require extremely clean graphene devices.

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